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24440

Q1-a)

There is a data hazard (Alu result) on line 2 as the value of register t0 gets written by instruction 1 on the 5th cycle but the updated value is required at the 2nd cycle during instruction decode of the 2nd instruction.

Similarly there is again a data hazard on line 3 as it requires the updated value of t0 on the 3rd cycle but t0 gets updated on the 5th cycle.

Q1 -b)

Data hazard (Alu result) in line 3 as t0 gets updated at the 6th cycle by the 2nd instruction but the updated value is required at the 4th cycle by the 3rd instruction.

Data hazard in line 4 as the value from t1 has not been received yet from memory and is required by the 4th instruction before.

Q1-c)

Data hazard in line 2 as t1 gets written back in the 5th cycle but is required by the 2nd instruction in the 3rd cycle.

Control hazard on line 4 as the 5th line will start to run even though the 4th instruction has not finished, and it is not necessary that the next instruction will always be the 5th line rather it can also be the line where the loop label is present.

Q2

Without pipeline:

Processor1: 350 + 450 + 400 + 555 + 150 = 1900ps

Processor2: 250 + 200 + 170 + 240 + 190 = 1050ps

With pipelining:

Processor1: 550 + 20 = 570ps

Processor2: 250 + 20 = 270ps

Q3

For processor 1 if we split MEM stage into 2 halves now the slowest stage will become ID with 450ps time hence the cycle time now becomes 470ps from 570ps.

For processor 2 if we split IF stage into 2 halves now the slowest stage will become ID with 240ps time hence the cycle time now becomes 260ps from 270ps.